Data Converters

Технически семинар
гр. Хисаря
Contents:

• Short product line update
• ADC architectures
  - SAR
  - Pipeline
  - Flash
  - Delta-Sigma / Modulator and Decimation
• ADC – Oversampling – when and why
• DAC architectures
  - R-2R
  - Resistor string
  - Voltage (current) source multiplying DAC
  - Current steering DAC
• Tools and Resources
The Signal Chain…

The Real World
- Temperature
- Pressure
- Position
- Speed
- Flow
- Humidity
- Sound
- Light
- Identification

#1 Amplifier
#2 Data Converter

#1 Interface
#2 Embedded Processing

Wireless Connectivity
Clocks & Timing
#1 Logic

#1 Amplifier
#2 Data Converter
## TI Data Converters At a Glance...

### Analog to Digital Converters

Select an option below to see more parts

<table>
<thead>
<tr>
<th>Analog to Digital Converters (Data Converters)</th>
<th>Sample Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution Bits</td>
<td>&lt; 100kSPS</td>
</tr>
<tr>
<td>31</td>
<td>100kSPS</td>
</tr>
<tr>
<td>24</td>
<td>1kSPS</td>
</tr>
<tr>
<td>22</td>
<td>10kSPS</td>
</tr>
<tr>
<td>20</td>
<td>100kSPS</td>
</tr>
<tr>
<td>18</td>
<td>500kSPS</td>
</tr>
<tr>
<td>16</td>
<td>1MSPS</td>
</tr>
<tr>
<td>14</td>
<td>10MSPS</td>
</tr>
<tr>
<td>13</td>
<td>50MSPS</td>
</tr>
<tr>
<td>12</td>
<td>100MSPS</td>
</tr>
<tr>
<td>11</td>
<td>1GSPS</td>
</tr>
<tr>
<td>10</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td></td>
</tr>
</tbody>
</table>
## Digital to Analog Converters

Select an option below to see more parts

<table>
<thead>
<tr>
<th>Resolution (Bits)</th>
<th>1</th>
<th>2</th>
<th>4</th>
<th>8</th>
<th>10MSPS to 499MSPS</th>
<th>&gt;=500MSPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>●</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>●</td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>16</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
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<td>14</td>
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<td>●</td>
<td>●</td>
<td>●</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
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<td></td>
</tr>
<tr>
<td>8</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td>●</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
TI Data Converters At a Glance…

TI offers a variety of data converters, both ADCs and DACs to fit all customer specific applications.

ADC solutions that provide high accuracy and resolution, fast signal processing, multiple analog inputs and low power.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>8 – 24 Bits</td>
</tr>
<tr>
<td># of Channels</td>
<td>1 – 24 Channels</td>
</tr>
<tr>
<td>Sampling Rate</td>
<td>10 SPS – 5 GSPS</td>
</tr>
<tr>
<td>Power</td>
<td>200µW – 4.4W</td>
</tr>
<tr>
<td>INL</td>
<td>± 0.09 LSB – ±10 LSB</td>
</tr>
<tr>
<td>SNR</td>
<td>40dB – 111 dB</td>
</tr>
<tr>
<td>SFDR</td>
<td>42 dB – 100 dB</td>
</tr>
<tr>
<td>Interface</td>
<td>SPI, I^2^C, Parallel, LVDS, JESD204B</td>
</tr>
<tr>
<td>Size</td>
<td>1.5x1.5mm – 19x19mm (WxL)</td>
</tr>
</tbody>
</table>

DAC solutions that provide high precision, fast speed, low settling time and audio optimized outputs.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>8 – 20 Bits</td>
</tr>
<tr>
<td># of Channels</td>
<td>1 – 16 Channels</td>
</tr>
<tr>
<td>Sampling Rate</td>
<td>500 SPS – 2.5 GSPS</td>
</tr>
<tr>
<td>Settling Time</td>
<td>400 pS – 2 mS</td>
</tr>
<tr>
<td>Power</td>
<td>15µW – 2W</td>
</tr>
<tr>
<td>INL</td>
<td>± 0.128 LSB – ± 65 LSB</td>
</tr>
<tr>
<td>Output Type</td>
<td>Current, Voltage (Buffered and Unbuffered)</td>
</tr>
<tr>
<td>Interface</td>
<td>SPI, I^2^C, Parallel, LVDS, JESD204B</td>
</tr>
<tr>
<td>Size</td>
<td>1.5x1.5mm – 14x52mm (WxL)</td>
</tr>
</tbody>
</table>
ADC Architectures…

ΔΣ – Delta Sigma
Or Sigma Delta
(Oversampling)

Converter Resolution (bits)

Conversion Rate

10
100
1K
10K
100K
1M
10M
5G

SPS

SAR
Successive Approximation

Pipeline
### ADC Architectures...

<table>
<thead>
<tr>
<th>Features</th>
<th>SAR</th>
<th>Delta-Sigma</th>
<th>Pipeline</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cost</td>
<td>$0,53 USD – 48,25 USD</td>
<td>$0,90 USD – 299,00 USD</td>
<td>$3,00 USD – 1079,82 USD</td>
</tr>
<tr>
<td>Power</td>
<td>Scales w/ Sample Rate</td>
<td>Constant</td>
<td>Constant / Scaled With Sample Rate</td>
</tr>
<tr>
<td>Package Size</td>
<td>Smaller</td>
<td>Larger</td>
<td>Larger</td>
</tr>
<tr>
<td>Resolution</td>
<td>Lower</td>
<td>Higher</td>
<td>Lower</td>
</tr>
<tr>
<td>Speed</td>
<td>Higher</td>
<td>Lower</td>
<td>Highest</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>Medium</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Latency</td>
<td>Low</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>Application</td>
<td>Motor Control/Positioning,</td>
<td>Medical (ECG, EEG, Blood Pressure, etc.),</td>
<td>Wireless/Wireline Communications,</td>
</tr>
<tr>
<td></td>
<td>Industrial Automation,</td>
<td>Audio, Test and Measurement, Motor Control</td>
<td>Medical Imaging, Radar Systems,</td>
</tr>
<tr>
<td></td>
<td>Test and Measurement</td>
<td></td>
<td>Data Acquisition</td>
</tr>
</tbody>
</table>

ADC Architectures...
ADC Checklist… To find the right ADC

Architecture? \( \Delta \Sigma \), SAR or Pipeline?

**SPEED (Sample Rate)** _____ and **RESOLUTION** ____ bits

**Analog Input** \( A_{in} \)

**Reference Voltage** \( V_{Ref} \) _____

**Analog Supply Voltage** \( AVDD \) _____

**Digital Supply Voltage** \( DVDD \) _____

**Digital Output** \( D_{OUT} \)

**Number of Channels** _____

Muxed or Simultaneous

Single Ended or Differential

Unipolar or Bipolar

**Input Voltage Range** _____

**Interface:**

Serial/SPI

I\(^2\)C

Parallel

LVDS: Serialized or Parallel

JESD204B
Architectures: Speed, Resolution, and Latency Analogy

*Trying to handle the truth*

(note: deepness of color is resolution and no converters were hurt for this example)

**Delta Sigma**
- 16 to 24 bits of resolution
- Typically Slow 10SPS to 105kSPS
- Long Latency
- If I was a camera I would have my aperture open longer

**SAR**
- 8 to 18 bits of resolution
- ~50kSPS to 4MSPS
- No latency
- If I was a camera I would have fast shutter speed

**Pipeline**
- 8 to 14 bits of resolution
- Up to over 200 MSPS
- Some clock cycle latency
- I want to be a video camera when I grow up
ADC – Successive Approximation Register (SAR) Architecture

- An “N” bit SAR converter takes N cycles to complete a conversion.
- Think “Binary Search”. From most to least significant bit (MSB to LSB) simple compare functions are done and, when a bit is a 1, that amount of voltage is subtracted from the input signal.
- SAR’s are workhorse converters… easy to use… simple to understand… but are limited in both resolution and speed.
- TI has MANY SAR ADCs!
Latency: SARs have none ...

OK, just a little

**ADS7881**
12 bits 4MSPS

If it was a 12 bit pipeline with 2 bits/stage, you would need:

$150 \, \eta s \, \text{Conv t Delay} = 6.6\text{MSPS} \times 6 \, \text{clock cycle delay = 40MSPS}$
Pipeline converters are another high speed architecture. Several lower resolution converters are put together to result in a fast conversion time. Generally lower power and lower cost than Flash converters, the main disadvantage of a Pipeline converter is that it takes as many clock cycles as there are stages to output the data resulting in latency.

**TI has many Pipeline converters!**
ADC – Pipeline Architecture (Flash ADC)
ADC – Pipeline Architecture

Data Latency
The sample must propagate through the entire pipeline before all its bits are available for combining in the digital-error-correction logic, data latency is associated with pipelined ADCs.
Analog Input Bandwidth of a Pipeline ADC

![Graph showing the input frequency vs. gain in dBFS for ADS5421, a 14-bit, 40-MSPS Pipeline ADC. The Full-power BW (FPBW) is approximately 550 MHz.]

**ADS5421**
14-bit, 40-MSPS Pipeline ADC

FPBW approx. 550 MHz

Full-power BW
Delta-Sigma Overview

• What is a delta-sigma ADC?
  – A 1-bit converter that uses oversampling (can be multi-bit) – No DNL
  – “Delta” = comparison with 1-bit DAC
  – “Sigma” = integration of the Delta measurement

• What is the advantage of delta-sigma?
  – Essentially digital parts which result in low cost
  – High resolution

• What are the disadvantages?
  – Limited frequency response
  – Most effective with continuous inputs
  – Latency
The Delta-Sigma Modulator

Delta

Signal input, $X_1$

Difference Amp

Sigma

$X_2$

Integrator

$X_3$

Comparator

(1-bit ADC)

$X_4$

1-bit DAC

To Digital Filter

$X_5$
Delta-Sigma Overview

Benefits of oversampling:

1. Relaxed antialiasing filter requirements – easier to design

\[ f_N = \text{Nyquist frequency} = 2f_m \]
Delta-Sigma Overview

Benefits of oversampling:

2. The resulting noise power is spread evenly over the complete spectrum.

Band of interest
The Frequency Domain

Frequency

Power

Signal amplitude

SNR = 6.02N + 1.76dB ; (for an N-bit ADC Sine wave input)

Quantization Noise

Average noise floor (flat)

FFT

Frequency

F_s / 2

F_s
Tests / Oversampling

(Quantization error)

\[ e_q \leq \frac{\Delta}{2} \]

\[ e_{RMS}^2 = \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e_q^2 \frac{1}{\Delta} \, de = \frac{\Delta^2}{12} \]

\[ e_{RMS}^2 = \frac{V_{REF}^2}{12 \cdot (2^N)^2} \]

\[ n_0^2 = \frac{e_{RMS}^2}{OSR} \]

\[ n_0 = \frac{V_{REF}}{2^N \cdot \sqrt{OSR} \cdot \sqrt{12}} \]

\[ OSR = 1 \]

\[ SNR = 20 \log \frac{V_{RMS}}{V_{n_0}} = 20 \log \frac{2^N \sqrt{12}}{2\sqrt{2}} = 20 \log(2^N \cdot 1,2247) \]

\[ SNR = 6,02 \cdot N + 1,76 \]
Oversampling by K Times

Oversampling by K times

\[ \text{SNR} = 6.02N + 1.76 \text{dB} ; \text{ (for an N-bit ADC Sine wave input)} \]

Same total noise, but spread over more frequencies

Frequency

FFT

Power

Average noise floor

\[ k \frac{F_S}{2} \to k F_S \]
The Digital Filter

- **Ideal digital filter response**

  - Oversampling by $K$ times
  
  
  \[
  \text{SNR} = 6.02N + 1.76\text{dB} + 10 \log(F_s/2*\text{BW})
  \]

- **Noise removed by filter**

  - Frequency range: $0$ to $k F_S / 2$

- **Power**

  - $F_X$ to $F_S$ for $X = 0, 1, \ldots, k - 1$
Noise-Shaped Spectrum

The integrator serves as a highpass filter to the noise.

The result is noise shaping

\[ \text{SNR} = 6.02N + 1.76\text{dB} \]
Delta-Sigma Overview

Benefits of oversampling:

3. The integrator serves as a high-pass filter to the noise, i.e. noise shaping.

Signal amplitude

Digital filter response

HF noise removed by the digital filter

Power

$k F_s / 2$  \hspace{2cm}  $k F_s$
Delta-Sigma Overview

Noise shaping

Note: Higher order Noise Shaper has less baseband noise

filtered in digital domain
1\textsuperscript{st} order $\Delta \Sigma$ Modulator
2\textsuperscript{nd} order $\Delta \Sigma$ modulator structure

- Converts the analog input signal into a single bit data stream with the pulse width being proportional to the input voltage
- Moves the quantization noise to higher frequencies (noise shaping)
3rd order $\Delta\Sigma$ Modulator
Averaging Filters

In this case, 4 samples of the 1-bit data were averaged, but any number of samples could have been chosen.
Averaging Filters

Digital decimation filter operation (example – 7 samples / bit )

Output from one bit ADC:

0 0 1 0 1 1 0 0 1 0 1 0 1 1 1 1 0 1 0 1 1 1 0 1 ……

4 x 0  3 x 0  2 x 0  3 x 0
3 x 1  4 x 1  5 x 1  4 x 1

i.e. 0  i.e. 1  i.e. 1  i.e. 1

Output decimation filter (÷7)
0 1 1 1

Decimation, or “rate reduction” filter.
i.e. averages the values and produces n-bit result at a lower frequency.
**AC Specs**

**SNR (Signal-to-Noise Ratio)** –

- RMS value representing the ratio of the amplitude of the desired signal to noise power below one half the sampling frequency.
- Measure of the strength of a signal to background noise.
- Contributes to the overall dynamic performance of the device at higher frequencies and affects the linearity at those frequencies.
- In the audio world, a low signal-to-noise ratio means the device has lots of hiss and static, while a high rating means clear-sounding audio.

**THD (Total Harmonic Distortion)** –

- The ratio of the sum of the powers of all harmonic frequencies above the fundamental frequency to the power of the fundamental frequency.
- THD is usually expressed in dB.
AC Specs

**ENOB (Effective Number Of Bits)** -

• The number of bits achieved in a real system.

• Is another way of specifying the SNR.

• ENOB = (SNR-1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this ENOB number of bits.

**SFDR (Spurious Free Dynamic Range)** -

• The headroom available in an FFT plot.

• It is the distance in dB between the fundamental input and the worse spur.
Tests / Oversampling

**Definitions:**
Експериментатор : Физик, който експериментира.
Теоретик: Физик, който НЕ експериментира.

**Oversampling:**
The process of sampling a signal with a signal with a sampling frequency significantly higher than the Nyquist rate.

**Oversampling benefits:**
1. Much easier Low Pass Filter
2. Improving of the SNR
Tests / Oversampling

Easier Low-pass filter

- Sampling frequency = $f_s$
- Sampling frequency = $2f_s$
- Oversampling ratio 2

Band of interest
Tests / Oversampling

Noise sources:

- Shot noise (статичен)
- Thermal noise
- Power Supply Variations
- VREF variations
- Phase Noise (sampling frequency jitter)
- Quantization noise

To reduce the noise:

- Thoughtful board layout
- baypass capacitor on VREF
- Oversampling and averaging
Tests / Oversampling

The input signal is a constant DC voltage

The system can be affected
From oversampling & averaging

i.e. If the combined sources of noise in the resultant ADC codes approximates White noise, then oversampling & averaging is a good idea.

- The noise is correlated
- Non-linear TF (PS noise, poor INL,…)

The oversampling & averaging
May not be helpful
Tests / Oversampling

**Sensor** → **Input interface** → **OpAmp** → **10-bit ADC** → **Oversampling & Averaging**

**EXAMPLE:**
MSP430F1232
Incl. 10-bit ADC - 200ksps, internal Vref=2.5V, 100ppm/°C
TL084ID – JFET, IIB = 30pAtyp, THD 0.003%, GBW = 3MHz

OpAmp role:
• Amplification/attenuation – scaling Vin to ADC input
• DC offset or level shifting
• Filtering
• Buffering (very, very, very high Zin)
  - impedance matching – ADC in may load the source, affecting it
  - reducing the effect of Cout (ADC Sample and Hold is a cap load)
  - single-ended to differential
Tests / Oversampling

FFT PLOT

SNR=53.1553
SINAD=46.771
SFDR=49.9653
THD=-47.9057
numpt=4096
tck[MHz]=0.002048

MATLAB 6.0 (late autumn 2005)
# Tests / Oversampling

## EXAMPLE Test Results

### Gain = 1, Full scale range

<table>
<thead>
<tr>
<th>OSR</th>
<th>1</th>
<th>2</th>
<th>4</th>
<th>8</th>
<th>16</th>
<th>24</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNR</td>
<td>58.1412</td>
<td>60.987</td>
<td>63.8621</td>
<td>66.884</td>
<td>70.0604</td>
<td>70.8278</td>
<td>71.4458</td>
</tr>
<tr>
<td>ENOB</td>
<td>9.36</td>
<td>9.83</td>
<td>10.32</td>
<td>10.82</td>
<td>11.35</td>
<td>11.47</td>
<td>11.57</td>
</tr>
</tbody>
</table>

### Gain = 32, Full scale range

<table>
<thead>
<tr>
<th>OSR</th>
<th>1</th>
<th>2</th>
<th>4</th>
<th>8</th>
<th>16</th>
<th>24</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNR</td>
<td>53.4286</td>
<td>56.6624</td>
<td>59.6724</td>
<td>63.7367</td>
<td>66.9566</td>
<td>67.5586</td>
<td>69.5452</td>
</tr>
</tbody>
</table>

### Gain = 235, Full scale range

<table>
<thead>
<tr>
<th>OSR</th>
<th>1</th>
<th>2</th>
<th>4</th>
<th>8</th>
<th>16</th>
<th>24</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNR</td>
<td>53.0249</td>
<td>54.6156</td>
<td>56.4216</td>
<td>58.4082</td>
<td>60.0756</td>
<td>60.5152</td>
<td>61.4182</td>
</tr>
<tr>
<td>ENOB</td>
<td>8.51</td>
<td>8.78</td>
<td>9.08</td>
<td>9.41</td>
<td>9.69</td>
<td>9.76</td>
<td>9.91</td>
</tr>
</tbody>
</table>

### Gain = 420, Full scale range

<table>
<thead>
<tr>
<th>OSR</th>
<th>1</th>
<th>2</th>
<th>4</th>
<th>8</th>
<th>16</th>
<th>24</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNR</td>
<td>53.1512</td>
<td>53.9534</td>
<td>54.9166</td>
<td>55.8196</td>
<td>56.6152</td>
<td>56.7828</td>
<td>57.3848</td>
</tr>
</tbody>
</table>
Tests / Oversampling

EXAMPLE Test Results

ENOB

Gain=1
Gain=32
Gain=235
Gain=420

OSR

0 5 10 15 20 25 30 35
TI DAC Technologies

Instrumentation and Measurement
Typically for Calibration

Industrial
Settling Time (µs)
Number of Output DACs
Resistor String – Inexpensive
R-2R – More accurate -Trimmed at final test
Typically Voltage out
MDAC’s (dig control gain/atten, Waveform gen.)

High Speed Video and Communication
Update rate (MSPS)
Typically 1 Output but a few 2 Output
Current out

Resistor String
& R-2R

Current Steering

Settling Time - µs

1/Update Rate

Setting time
## DAC Architectures

<table>
<thead>
<tr>
<th>Features</th>
<th>String</th>
<th>R-2R</th>
<th>MDAC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cost</td>
<td>$</td>
<td>$$</td>
<td>$$$</td>
</tr>
<tr>
<td>Power</td>
<td>Low</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>Package Size</td>
<td>Smaller</td>
<td>Larger</td>
<td>Larger</td>
</tr>
<tr>
<td>Resolution</td>
<td>Lower</td>
<td>Higher</td>
<td>Higher</td>
</tr>
<tr>
<td>Linearity</td>
<td>Bad</td>
<td>Good</td>
<td>Good</td>
</tr>
<tr>
<td>Settling Time</td>
<td>High</td>
<td>Medium</td>
<td>Low</td>
</tr>
<tr>
<td>Buffered</td>
<td>Integrated Buffer Built In</td>
<td>Optional Buffered/Unbuffered</td>
<td>No Buffer; Need External Buffer</td>
</tr>
<tr>
<td>Glitch Energy</td>
<td>Low</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>Application</td>
<td>Walkie-Talkie, ATM machines, Dome Control, 3-wire Field transmitter, PLC</td>
<td>MRI scanners, pulse oximetry, mass spectrometer</td>
<td>DC load, pulse oximetry</td>
</tr>
</tbody>
</table>
DAC Checklist... To find the right DAC

Architecture? Resistor String or Current Steering?

Settling Time _____ and RESOLUTION _____ bits

Reference Voltage VRef: Int or Ext

Analog Supply Voltage AVDD _____

Digital Supply Voltage DVDD _____

Digital Input D_IN

Interface:
Serial/SPI
I²C
Parallel
LVDS: Serialized or Parallel
JESD204B

Analog Output A_OUT

Voltage or Current Buffered or Unbuffered?
R-2R Architecture

- small. Only 2*N resistors required
- tight resistor matching required
- not inherently monotonic
Resistor String DAC Architecture

\[ V_{OUT} = V_{REF} \sum \left( \frac{b_i}{2^i} \right) \]
Typical Block Diagrams of a Resistor String DAC

(a) Buffered output

(b) Fixed gain
A Voltage source multiplying DAC

Fast.
Settling times of 100ns or less
A Current source multiplying DAC

1mA 0.5mA 0.25mA 0.125mA

MSB 0.5mA 0.25mA 0.125mA

LSB
Current Steering DACs

2\(^{N-1}\) Current Sources

Switches determined by digital input

\(I_{\text{out}} + I_{\text{out}'} = \text{const}\)
### ADCs

<table>
<thead>
<tr>
<th>Prefix</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADS1xxx</td>
<td>Delta-Sigma ADCs</td>
</tr>
<tr>
<td>ADS120x</td>
<td>Delta-Sigma Modulators</td>
</tr>
<tr>
<td>AMC1xxx</td>
<td>Isolated Delta-Sigma Modulator</td>
</tr>
<tr>
<td>ADS78xx/ADS8xxx</td>
<td>SAR/Nyquist ADCs</td>
</tr>
<tr>
<td>ADS4xxx/ADS5xxx/ADS6xxx</td>
<td>High-speed (&gt;10 MSPS)</td>
</tr>
<tr>
<td>AMC78xx</td>
<td>Integrated Precision ADCs and DACs</td>
</tr>
<tr>
<td>ADCxxxx/LMxxxxx</td>
<td>High-speed (&gt;10 MSPS)</td>
</tr>
<tr>
<td>TLC/TLV5xxx</td>
<td>Precision (&lt;=10 MSPS)</td>
</tr>
<tr>
<td>THSxxxxx</td>
<td>Precision (&lt;=10 MSPS)</td>
</tr>
<tr>
<td>ADCxxxx</td>
<td>Precision (&lt;=10 MSPS)</td>
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</table>

**Web site price:** 0.53 USD to 3299.49 USD

### DACs

<table>
<thead>
<tr>
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<tbody>
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<td>DAC1xxx</td>
<td>Delta-Sigma DACs</td>
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<tr>
<td>DACx5xx</td>
<td>String DACs</td>
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<tr>
<td>DAC76xx</td>
<td>R-2R DACs</td>
</tr>
<tr>
<td>DAC77xx</td>
<td>R2R High-voltage DACs</td>
</tr>
<tr>
<td>DAC88xx</td>
<td>Multiplying DACs</td>
</tr>
<tr>
<td>TLC/TLVxxx</td>
<td>String DACs</td>
</tr>
<tr>
<td>DAC5xxx/THS5xxx</td>
<td>High-speed DACs</td>
</tr>
<tr>
<td>DAC3xxx</td>
<td>High-speed DACs</td>
</tr>
<tr>
<td>AMC78xx</td>
<td>Integrated Precision ADCs and DACs</td>
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**Web site price:** 0.38 USD to 109 USD
# Tools & Resources…

## Design Tools

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<th>Tool</th>
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<tbody>
<tr>
<td>Anti-Aliasing Calculation Tool for A to D Converters</td>
</tr>
<tr>
<td>ADC Harmonic Calculator</td>
</tr>
<tr>
<td>Op Amp to ADC Circuit Topology Calculator</td>
</tr>
<tr>
<td>Jitter and SNR Calculator for ADCs</td>
</tr>
<tr>
<td>Loop Filter Calculation Tool</td>
</tr>
</tbody>
</table>

## TI Designs

- Low Cost Loop-Powered 4-20mA Transmitter EMC/EMI Tested
- Analog Front End (AFE) for Merging Units and Multi-Function Protection Relays
- Digitally Tunable MDAC Based State Variable Filter
Tools & Resources...

**Precision Data Converters**

**Technical Support and Resources**

**TI Precision Designs™**—TI Precision Designs is a library of complete board-and-system level circuits designed to help engineers quickly evaluate and customize their systems while expanding their analog knowledge base. Three levels of designs are offered - Reference, Verified and Certified - providing a combination of theory, methodology, simulation, tested results, and design files from the desks of our analog experts.

**TI E2E™ Community**—Open network of > 50,000 engineers and TI experts who collaborate by asking and answering technical questions and solving problems.

**Sensor AFE WEBENCH® Software**—Easy to use online design tool that allows you to select sensors, configure signal path, evaluate performance and move rapidly to prototyping.

**ADCPro™**—Modular software system for evaluating ADCs without the need for expensive logic analyzers and complex analysis routines.

**IBIS Models**—I/O Buffer Specification is an industry standard, fast and accurate behavioral method of modeling input/output buffers based on V/I curve data derived from measurement or full circuit simulation. These are widely used for signal integrity analysis on system boards and can be used by any simulators/EDA tools in the industry.

**TINA-TI™**—is an easy-to-use, powerful circuit simulation tool based on a SPICE engine, and Texas Instruments is the industry's first and currently only company to incorporate a SAR ADC front-end macromodel into a SPICE simulation tool.
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  - Theory
  - Calculations
  - Simulation
  - Design methodology

Verified Designs
- Reference Designs+
  - Schematics
  - Bench results
  - Layout and design files

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- Verified Designs+
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  - Simulation
  - Design Methodology

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- Reference +
  - Schematics
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- Verified +
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<table>
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<tr>
<th>Type</th>
<th>App Function</th>
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</thead>
<tbody>
<tr>
<td>Reference</td>
<td>Converter Reference Design, 0 to 5 V Input, 0 mA to 500 mA Output</td>
</tr>
<tr>
<td></td>
<td>High-Side V-I Converter, 0-2V to 0-100mA, 1% Full Scale Error</td>
</tr>
<tr>
<td></td>
<td>Bridge Tied Load (BTL) V-I Converter, 0.5-4.5V to +/-2A</td>
</tr>
<tr>
<td></td>
<td>Current Sensing Solution, 10uA-10mA, Low-side, Single Supply</td>
</tr>
<tr>
<td></td>
<td>AC Coupled Comparator Reference Design, Input 2kHz to 32MHz</td>
</tr>
<tr>
<td></td>
<td>Low-Level V-to-I Converter Reference Design, 0V to 5V input to 0uA to 5uA output</td>
</tr>
<tr>
<td></td>
<td>Analog PWM Generator 5V, 500kHz PWM Output</td>
</tr>
</tbody>
</table>

Sign up to receive email notifications when new Precision Designs are added.
Tools & Resources...

High Speed Data Converter Pro Software

(Active) DataConverterPro-SW

Description & Features  Technical Documents  Support & Training

Order Now

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<th>Part Number</th>
<th>Buy from Texas Instruments or Third Party</th>
<th>Status</th>
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<td>DATACONVERTERPRO-SW:</td>
<td>Download</td>
<td>ACTIVE</td>
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High Speed Data Converter Pro Software

Description

The High Speed Data Converter Pro GUI is a PC (Windows XP / 7 compatible) program designed to aid in evaluation of most TI high speed data converter and AFE platforms. Designed to support the entire TSW14xx series of data capture and pattern generation cards, including the TSW1400EVM and TSW14J56EVM, the High Speed Data Converter Pro GUI provides a powerful and quick solution for analyzing TI data converters in both the time and frequency domains, and with single-tone, multi-tone and modulated signal support. The GUI is also compatible with TI's Pattern Generation GUI for quick synthesis of single-tone, multi-tone and modulated signals. Users can also provide custom patterns to the GUI for loading to TI DACs, and CSV file exports from ADC captures are supported for external analysis.

Compatible with:

- 97 Design Kits & EVMs
- 122 Related devices

Designed to support the entire TSW14xx series of data capture and pattern generation cards, including the TSW1400EVM and TSW14J56EVM
Tools & Resources…
Tools & Resources…

Compatible with:
- 86 Design Kits & EVMs
- 119 Devices

capture and pattern generation card
Tools & Resources...

A block diagram of the TSW1400 EVM is shown in Figure 1.

Capture and pattern generation card
Tools & Resources...

Figure 10. TSW1400EVM Interfacing to the CMOS Connectors of an ADS62P49EVM

capture and pattern generation card
Figure 12. TSW1400 EVM Interfacing to a DAC EVM

capture and pattern generation card
Tools & Resources...

Compatible with:
- 21 Design Kits & EVMs
- 21 Devices

JESD204B

capture and pattern generation card
Tools & Resources...

Figure 2 shows a block diagram of the TSW14J56 EVM.

Compatible with:
- 21 Design Kits & EVMs
- 21 Devices

JESD204B

capture and pattern generation card
Tools & Resources…

Compatible with:

• 21 Design Kits & EVMs
• 21 Devices

JESD204B

capture and pattern generation card
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Figure 1. 430BOOST-ADS1118 BoosterPack Overview
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CONCLUSION...